FIG. 1

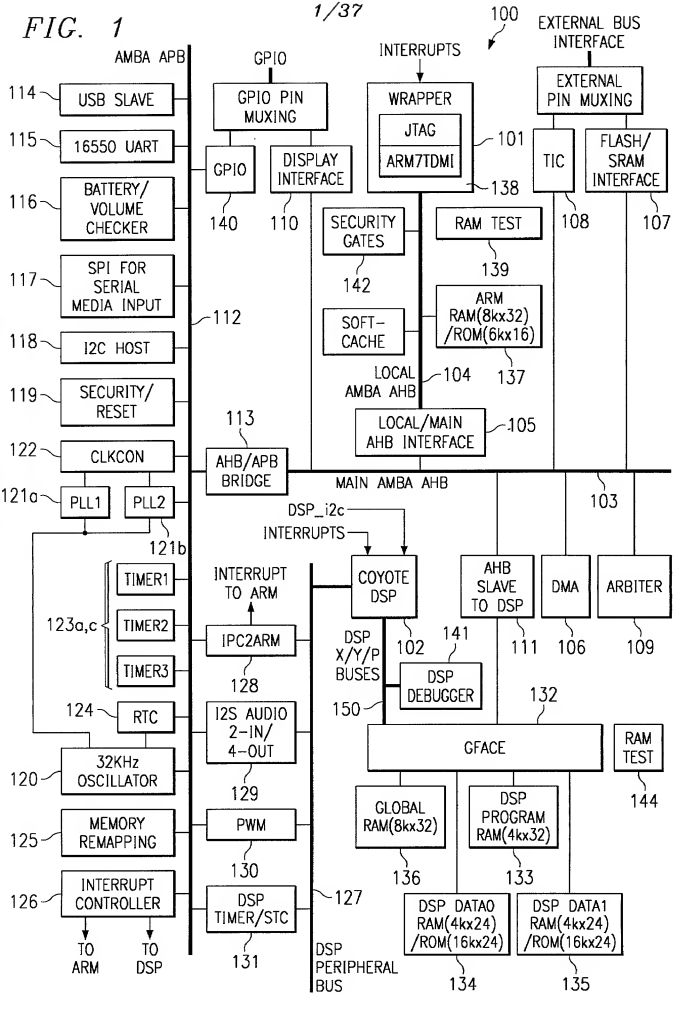
100
EXTERNAL BUS INTERFACE
AMBA APB
GPIO
INTERRUPTS
EXTERNAL PIN MUXING
114
USB SLAVE
GPIO PIN MUXING
WRAPPER
JTAG
ARM7TDMI
101
115
16550 UART
GPIO
DISPLAY INTERFACE
TIC
FLASH/ SRAM INTERFACE
138
116
BATTERY/ VOLUME CHECKER
140
110
SECURITY GATES
RAM TEST
108
107
117
SPI FOR SERIAL MEDIA INPUT
142
139
ARM RAM(8kx32) /ROM(6kx16)
112
SOFT-CACHE
118
I2C HOST
LOCAL AMBA AHB
104
137
119
SECURITY/ RESET
113
LOCAL/MAIN AHB INTERFACE
105
122
CLKCON
AHB/APB BRIDGE
MAIN AMBA AHB
103
121a
PLL1
PLL2
121b
DSP_i2c
INTERRUPTS
TIMER1
INTERRUPT TO ARM
COYOTE DSP
AHB SLAVE TO DSP
DMA
ARBITER
123a,c
TIMER2
IPC2ARM
DSP X/Y/P BUSES
102
141
111
106
109
TIMER3
128
DSP DEBUGGER
124
RTC
I2S AUDIO 2-IN/ 4-OUT
150
132
GFACE
RAM TEST
120
32KHz OSCILLATOR
129
144
GLOBAL RAM(8kx32)
DSP PROGRAM RAM(4kx32)
125
MEMORY REMAPPING
PWM
130
136
133
126
INTERRUPT CONTROLLER
DSP TIMER/STC
127
DSP DATA0 RAM(4kx24) /ROM(16kx24)
DSP DATA1 RAM(4kx24) /ROM(16kx24)
TO ARM
TO DSP
131
DSP PERIPHERAL BUS
134
135

FIG. 2A

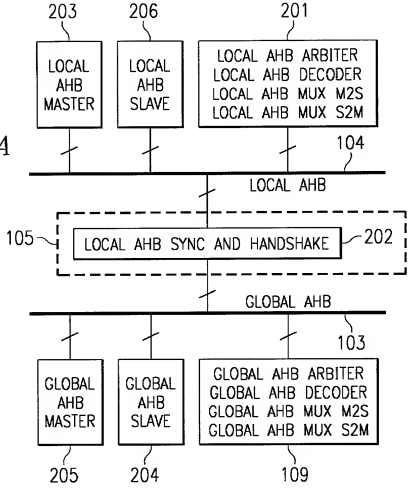
203
206
201
LOCAL AHB MASTER
LOCAL AHB SLAVE
LOCAL AHB ARBITER
LOCAL AHB DECODER
LOCAL AHB MUX M2S
LOCAL AHB MUX S2M
104
LOCAL AHB
105
LOCAL AHB SYNC AND HANDSHAKE
202
GLOBAL AHB
103
GLOBAL AHB MASTER
GLOBAL AHB SLAVE
GLOBAL AHB ARBITER
GLOBAL AHB DECODER
GLOBAL AHB MUX M2S
GLOBAL AHB MUX S2M
205
204
109

FIG. 3

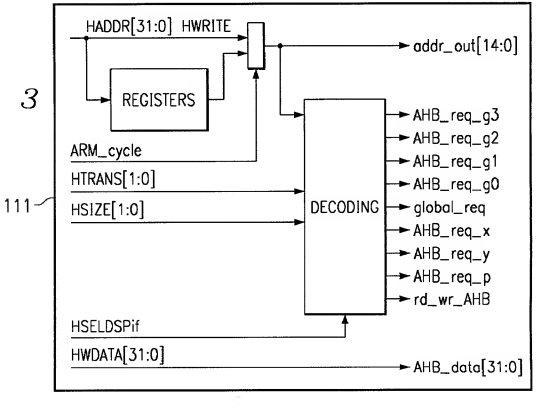
HADDR[31:0]
HWRITE
addr_out[14:0]
REGISTERS
ARM_cycle
HTRANS[1:0]
111
HSIZE[1:0]
DECODING
AHB_req_g3
AHB_req_g2
AHB_req_g1
AHB_req_g0
global_req
AHB_req_x
AHB_req_y
AHB_req_p
rd_wr_AHB
HSELDSPif
HWDATA[31:0]
AHB_data[31:0]

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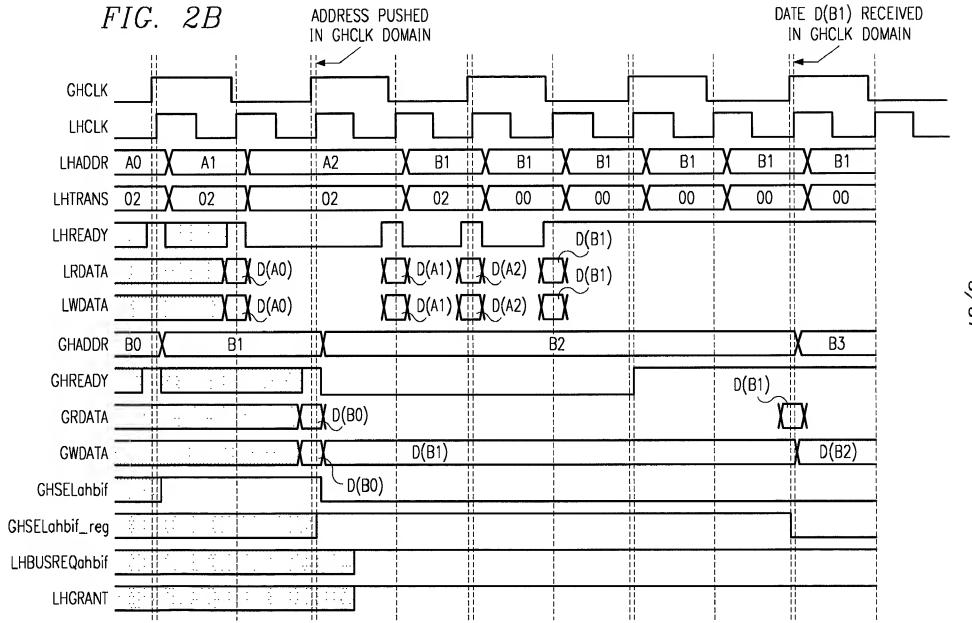
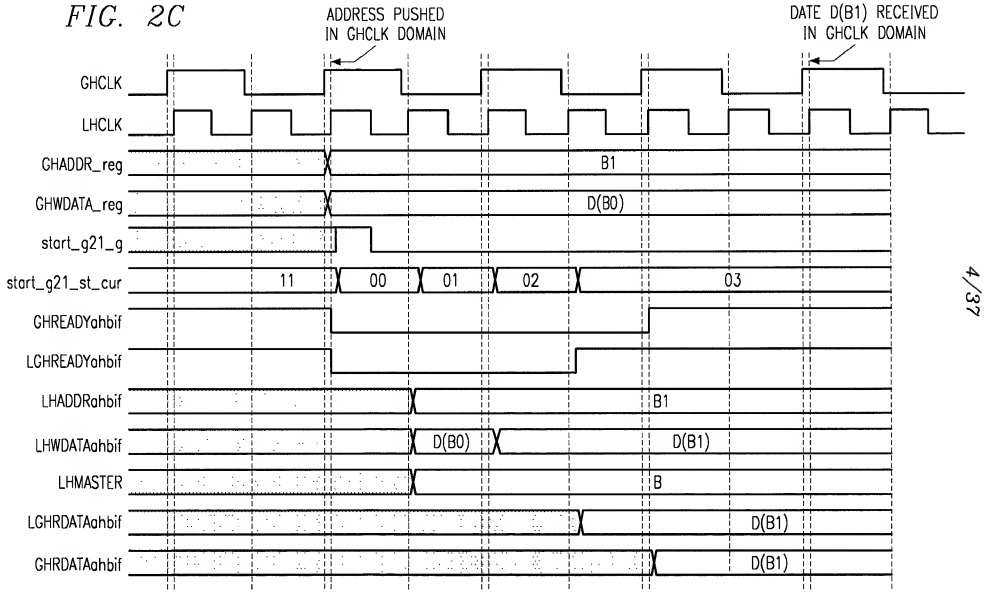
FIG. 2B



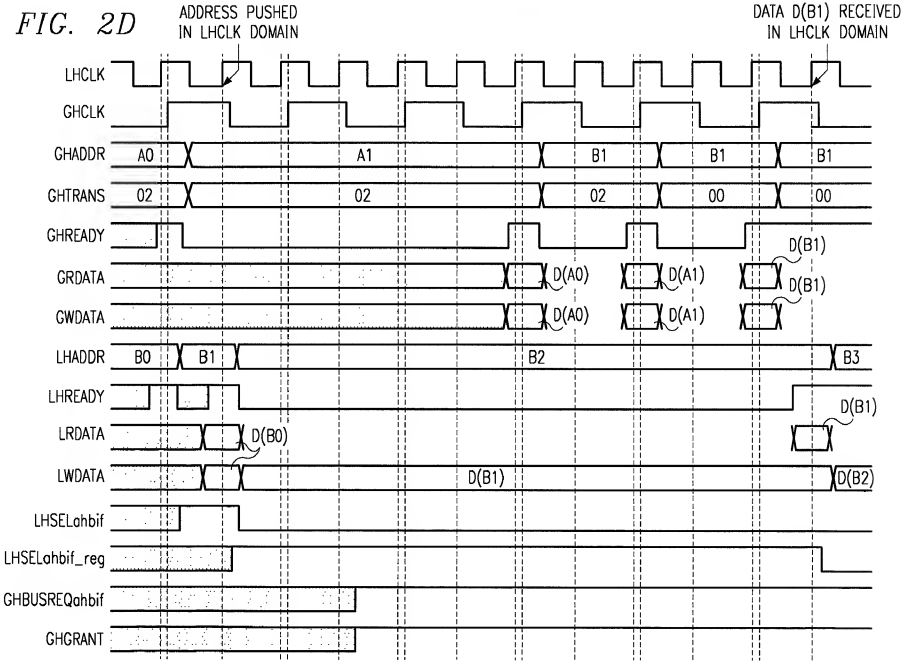
TOSTOO:2687290

FIG. 2C



T00760 26812860

FIG. 2D



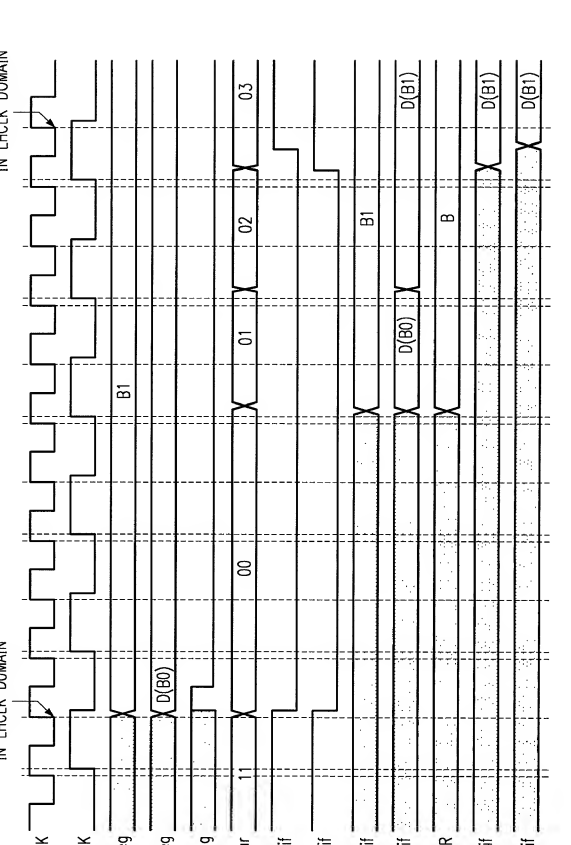

ADDRESS PUSHED IN LHCLK DOMAIN
DATA D(B1) RECEIVED IN LHCLK DOMAIN
LHCLK
GHCLK
LHADDR_reg
LHWDATA_reg
start_12g_g
start_12g_st_cur
LHREADYahbif
GLHREADYahbif
GHADDRahbif
GHWDATAahbif
GHMASTER
GLHRDATAahbif
LHRDATAahbif
B1
D(B0)
00
11
01
02
03
B
D(B1)

FIG. 2E

FIG. 4A

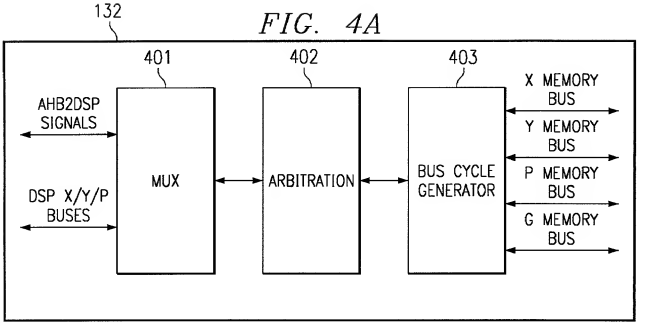

132
401
402
403
AHB2DSP SIGNALS
DSP X/Y/P BUSES
MUX
ARBITRATION
BUS CYCLE GENERATOR
X MEMORY BUS
Y MEMORY BUS
P MEMORY BUS
G MEMORY BUS

FIG. 4B

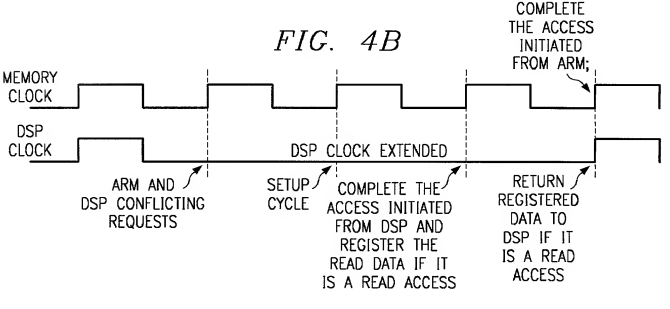

MEMORY CLOCK
DSP CLOCK
DSP CLOCK EXTENDED
COMPLETE THE ACCESS INITIATED FROM ARM;
ARM AND DSP CONFLICTING REQUESTS
SETUP CYCLE
COMPLETE THE ACCESS INITIATED FROM DSP AND REGISTER THE READ DATA IF IT IS A READ ACCESS
RETURN REGISTERED DATA TO DSP IF IT IS A READ ACCESS

FIG. 4C

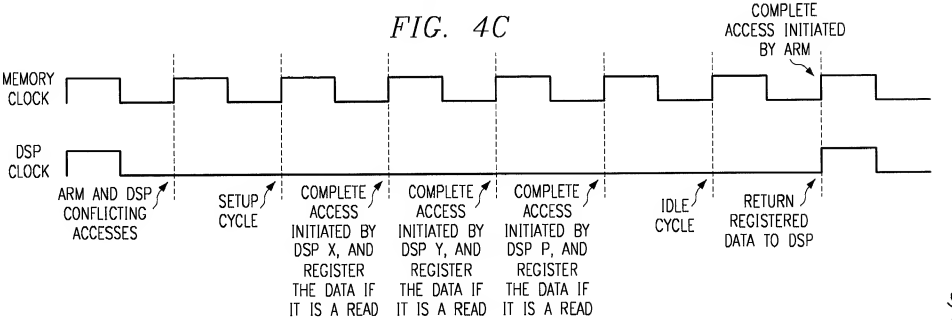
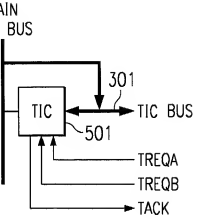

MEMORY CLOCK
DSP CLOCK
ARM AND DSP CONFLICTING ACCESSES
SETUP CYCLE
COMPLETE ACCESS INITIATED BY DSP X, AND REGISTER THE DATA IF IT IS A READ
COMPLETE ACCESS INITIATED BY DSP Y, AND REGISTER THE DATA IF IT IS A READ
COMPLETE ACCESS INITIATED BY DSP P, AND REGISTER THE DATA IF IT IS A READ
IDLE CYCLE
RETURN REGISTERED DATA TO DSP
COMPLETE ACCESS INITIATED BY ARM

FIG. 5


MAIN AHB BUS
301
TIC
TIC BUS
501
TREQA
TREQB
TACK

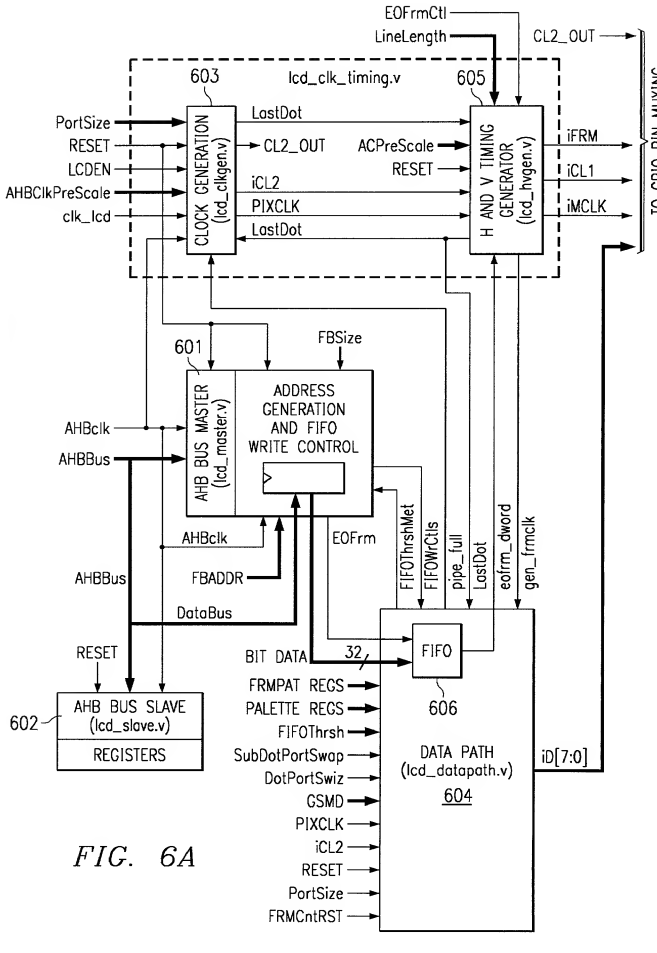

EOFrmCtl
LineLength
CL2_OUT
603
lcd_clk_timing.v
605
PortSize
RESET
LCDEN
AHBClkPreScale
clk_lcd
CLOCK GENERATION (lcd_clkgen.v)
LastDot
CL2_OUT
iCL2
PIXCLK
LastDot
ACPreScale
RESET
H AND V TIMING GENERATOR (lcd_hvgen.v)
iFRM
iCL1
iMCLK
TO GPIO PIN MUXING
601
FBSize
AHB BUS MASTER (lcd_master.v)
ADDRESS GENERATION AND FIFO WRITE CONTROL
AHBclk
AHBBus
AHBclk
AHBBus
FBADDR
DataBus
EOFrm
FIFOThrshMet
FIFOWrCtls
pipe_full
LastDot
eofrm_dword
gen_frmclk
RESET
BIT DATA
32
FIFO
606
602
AHB BUS SLAVE (lcd_slave.v)
REGISTERS
FRMPAT REGS
PALETTE REGS
FIFOThrsh
SubDotPortSwap
DotPortSwiz
GSMD
PIXCLK
iCL2
RESET
PortSize
FRMCntRST
DATA PATH (lcd_datapath.v)
604
iD[7:0]

FIG. 6A

FIG. 6B

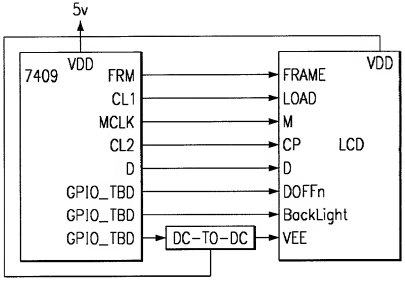
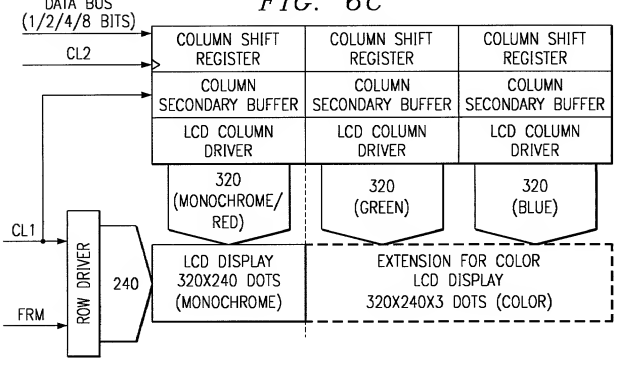

5v
7409
VDD
FRM
CL1
MCLK
CL2
D
GPIO_TBD
GPIO_TBD
GPIO_TBD
DC-TO-DC
VDD
FRAME
LOAD
M
CP
LCD
D
DOFFn
BackLight
VEE

FIG. 6C


DATA BUS
(1/2/4/8 BITS)
CL2
CL1
FRM
ROW DRIVER
240
COLUMN SHIFT REGISTER
COLUMN SHIFT REGISTER
COLUMN SHIFT REGISTER
COLUMN SECONDARY BUFFER
COLUMN SECONDARY BUFFER
COLUMN SECONDARY BUFFER
LCD COLUMN DRIVER
LCD COLUMN DRIVER
LCD COLUMN DRIVER
320 (MONOCHROME/ RED)
320 (GREEN)
320 (BLUE)
LCD DISPLAY 320X240 DOTS (MONOCHROME)
EXTENSION FOR COLOR LCD DISPLAY 320X240X3 DOTS (COLOR)

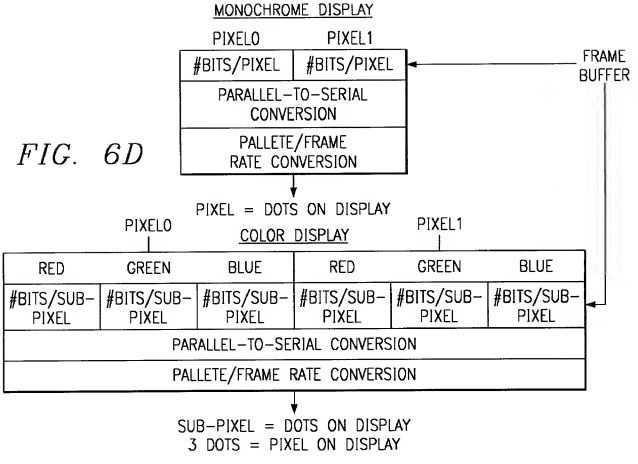

MONOCHROME DISPLAY
PIXEL0
PIXEL1
#BITS/PIXEL
#BITS/PIXEL
FRAME BUFFER
PARALLEL-TO-SERIAL CONVERSION
PALLETE/FRAME RATE CONVERSION
PIXEL = DOTS ON DISPLAY
PIXEL0
COLOR DISPLAY
PIXEL1
RED
GREEN
BLUE
RED
GREEN
BLUE
#BITS/SUB-PIXEL
PARALLEL-TO-SERIAL CONVERSION
PALLETE/FRAME RATE CONVERSION
SUB-PIXEL = DOTS ON DISPLAY
3 DOTS = PIXEL ON DISPLAY

FIG. 6D

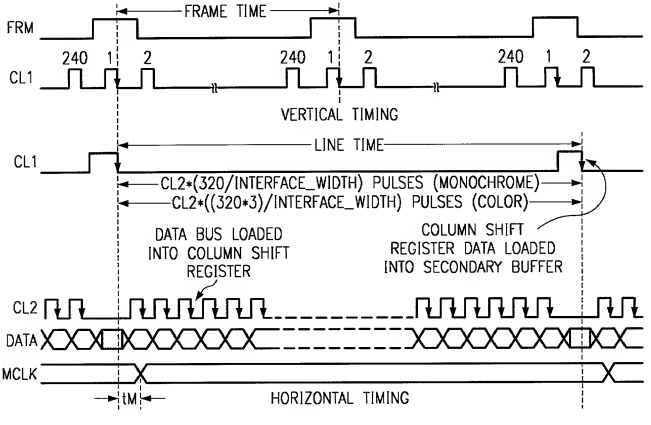
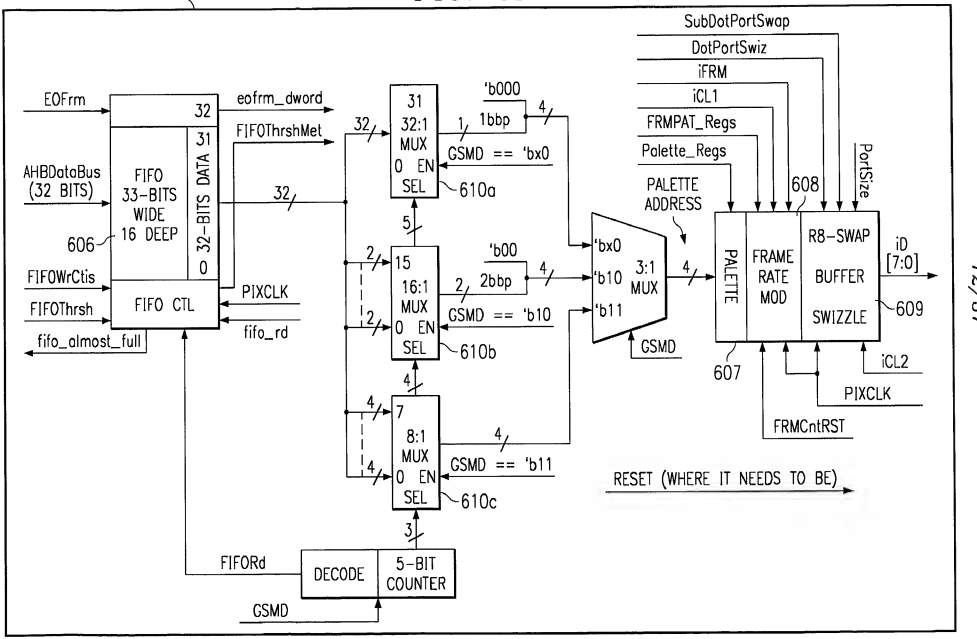

FRAME TIME
FRM
240
1
2
CL1
VERTICAL TIMING
LINE TIME
CL2*(320/INTERFACE_WIDTH) PULSES (MONOCHROME)
CL2*((320*3)/INTERFACE_WIDTH) PULSES (COLOR)
DATA BUS LOADED INTO COLUMN SHIFT REGISTER
COLUMN SHIFT REGISTER DATA LOADED INTO SECONDARY BUFFER
CL2
DATA
MCLK
tM
HORIZONTAL TIMING

FIG. 6E

FIG. 6F


604
SubDotPortSwap
DotPortSwiz
iFRM
iCL1
FRMPAT_Regs
Palette_Regs
PortSize
EOFrm
eofrm_dword
FIFOThrshMet
AHBDataBus (32 BITS)
FIFO 33-BITS WIDE 16 DEEP
32-BITS DATA
606
FIFOWrCtis
FIFOThrsh
FIFO CTL
PIXCLK
fifo_rd
fifo_almost_full
32:1 MUX
16:1 MUX
8:1 MUX
0 EN
SEL
610a
610b
610c
'b000
1bbp
GSMD == 'bx0
'b00
2bbp
GSMD == 'b10
GSMD == 'b11
'bx0
'b10
'b11
3:1 MUX
GSMD
PALETTE ADDRESS
608
PALETTE
FRAME RATE MOD
R8-SWAP BUFFER SWIZZLE
609
607
iD [7:0]
iCL2
PIXCLK
FRMCntRST
RESET (WHERE IT NEEDS TO BE)
FIFORd
DECODE
5-BIT COUNTER
GSMD

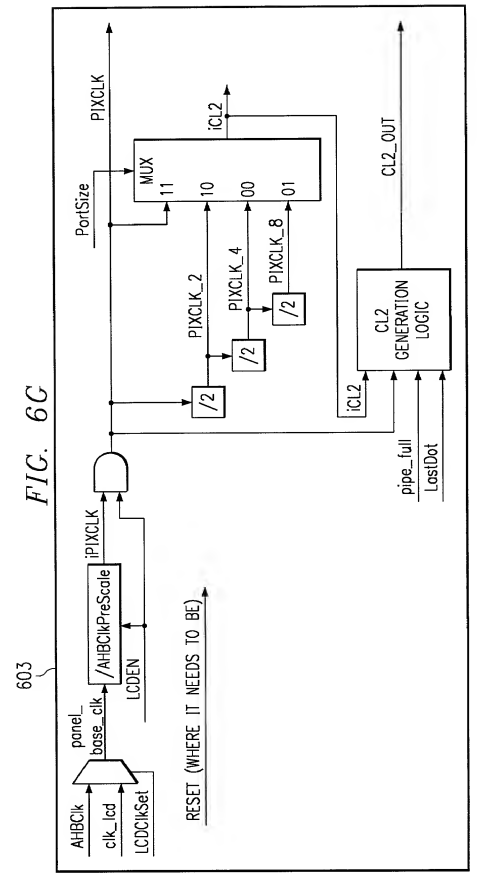

603
AHBClk
clk_lcd
LCDClkSet
panel_
base_clk
/AHBClkPreScale
iPIXCLK
LCDEN
RESET (WHERE IT NEEDS TO BE)
PortSize
PIXCLK
MUX
11
10
00
01
iCL2
PIXCLK_2
PIXCLK_4
PIXCLK_8
/2
/2
/2
iCL2
CL2
GENERATION
LOGIC
CL2_OUT
pipe_full
LastDot

FIG. 6C

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FIG. 6H

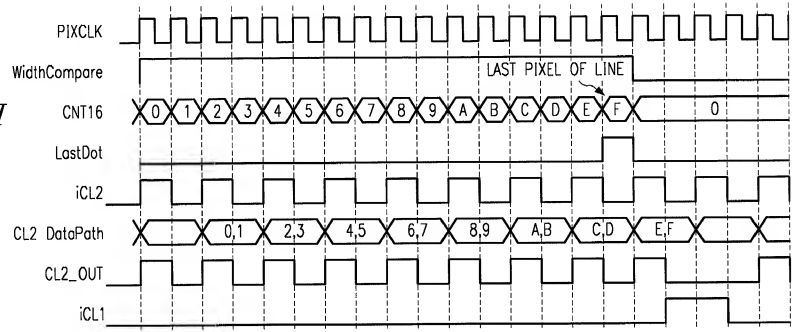

FIG. 6I

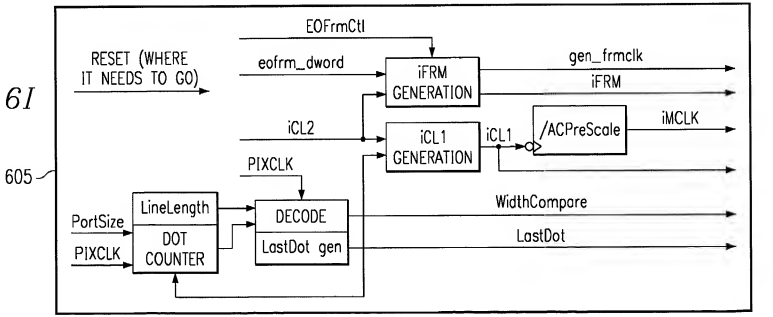

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FIG. 6J

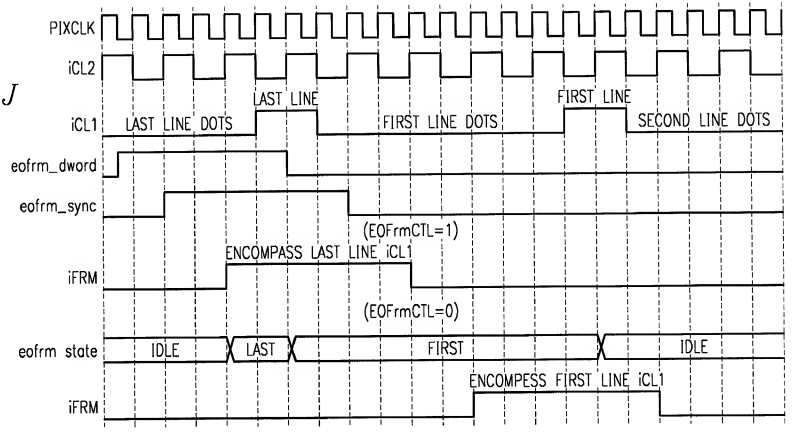

FIG. 6K

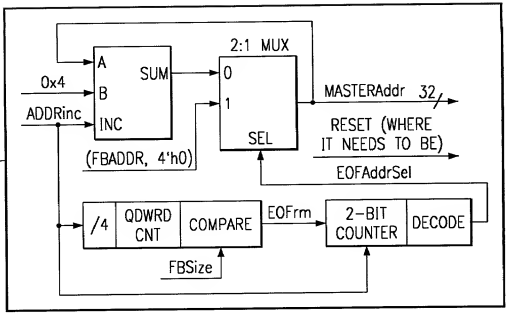

FIG. 17

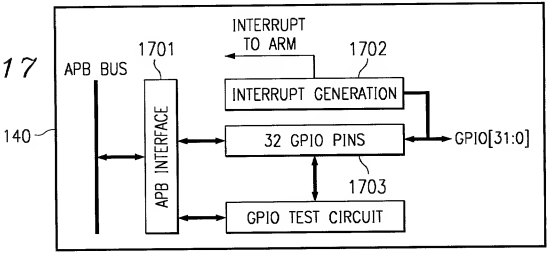

FIG. 18

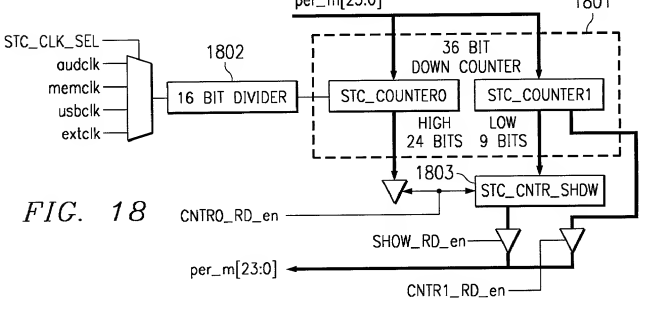

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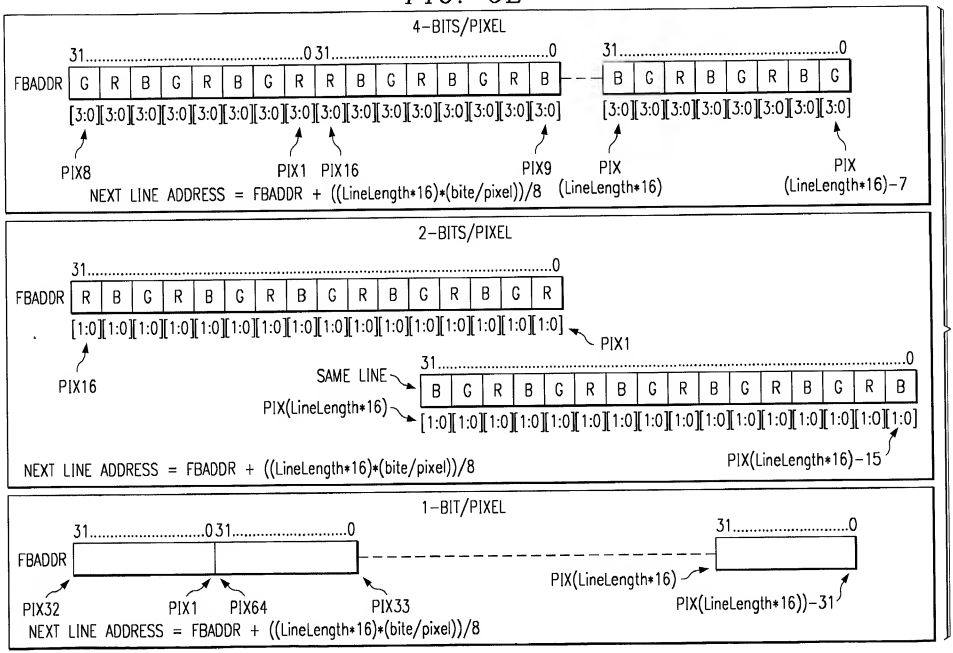
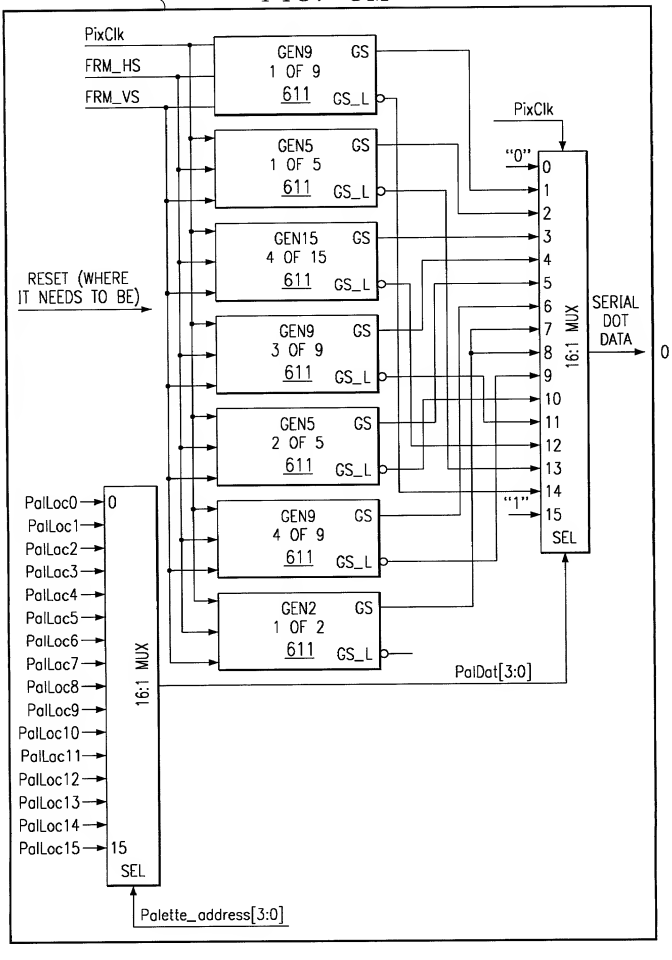
FIG. 6L



609

FIG. 6M


PixClk
FRM_HS
FRM_VS
GEN9 GS
1 OF 9
611 GS_L
GEN5 GS
1 OF 5
611 GS_L
GEN15 GS
4 OF 15
611 GS_L
GEN9 GS
3 OF 9
611 GS_L
GEN5 GS
2 OF 5
611 GS_L
GEN9 GS
4 OF 9
611 GS_L
GEN2 GS
1 OF 2
611 GS_L
RESET (WHERE IT NEEDS TO BE)
PixClk
"0"
"1"
16:1 MUX
SEL
SERIAL DOT DATA
0
PalDat[3:0]
PalLoc0
PalLoc1
PalLoc2
PalLoc3
PalLoc4
PalLoc5
PalLoc6
PalLoc7
PalLoc8
PalLoc9
PalLoc10
PalLoc11
PalLoc12
PalLoc13
PalLoc14
PalLoc15
16:1 MUX
SEL
Palette_address[3:0]

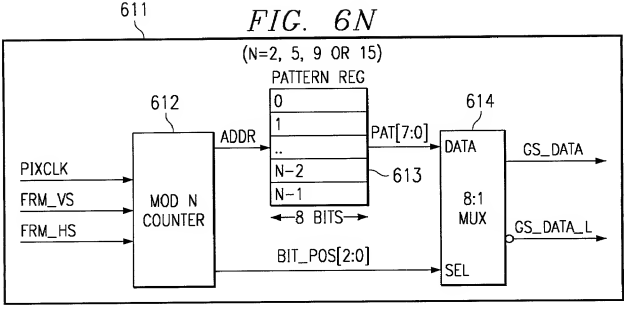


FIG. 6N

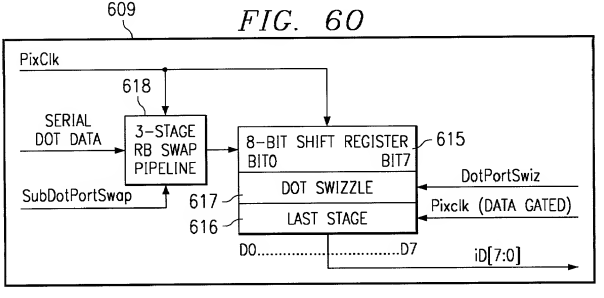


FIG. 6O

FIG. 6P

TIME (FROM THE SHIFT REGISTER POINT OF VIEW)

SubDotPortSwap=0

{BnGnRn}.....{B3G3R3}{B2G2R2}{B1G1R1}{B0G0R0}

SubDotPortSwap=1

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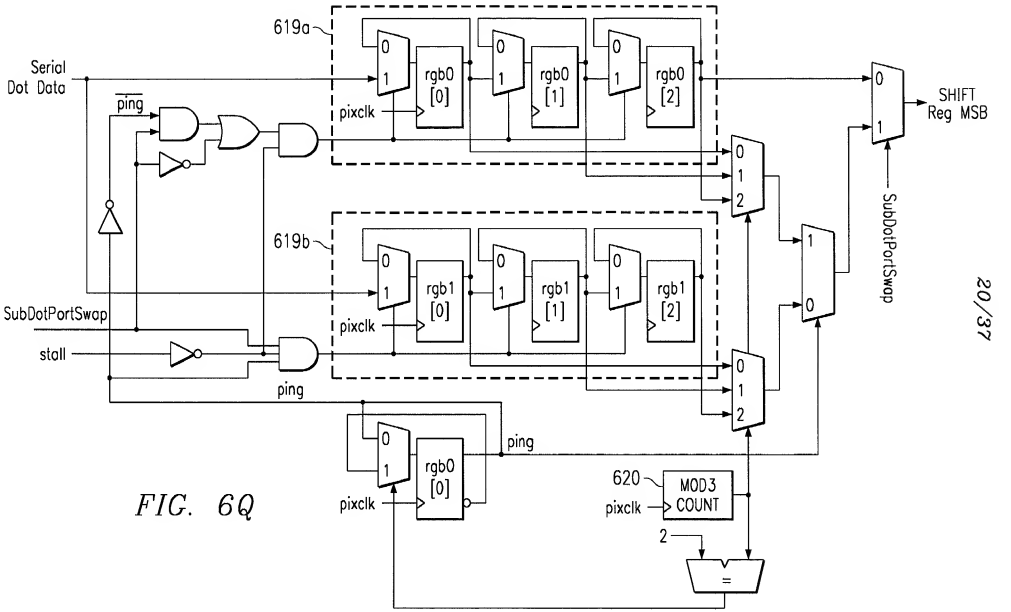


FIG. 6Q

FIG. 6R

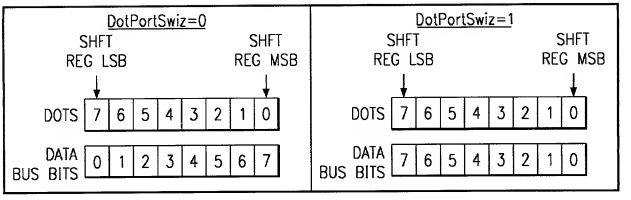


FIG. 6S

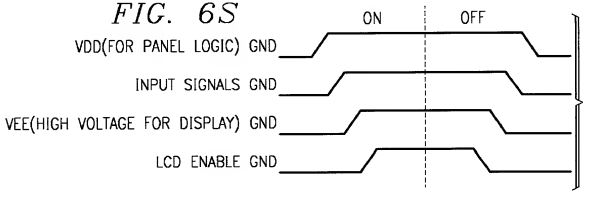


FIG. 7A

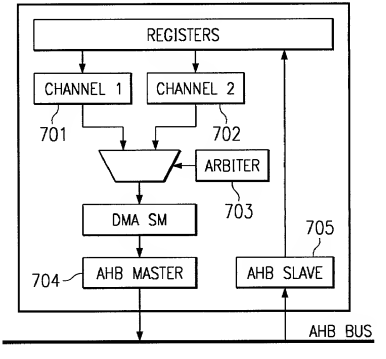


FIG. 7B

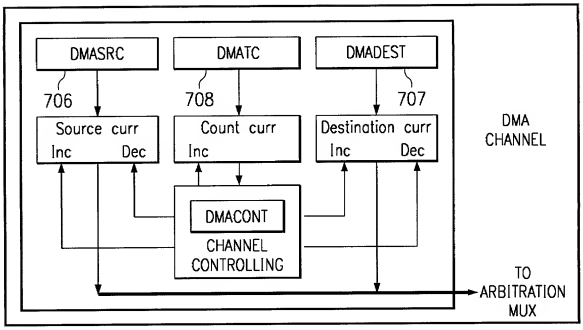

DMASRC
DMATC
DMADEST
706
708
707
Source curr
Inc
Dec
Count curr
Inc
Destination curr
Inc
Dec
DMA
CHANNEL
DMACONT
CHANNEL
CONTROLLING
TO
ARBITRATION
MUX

FIG. 8

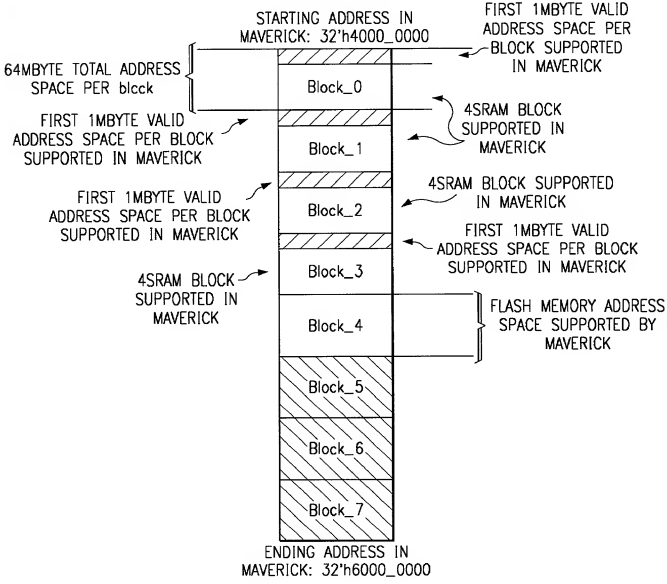

STARTING ADDRESS IN
MAVERICK: 32'h4000_0000
FIRST 1MBYTE VALID
ADDRESS SPACE PER
BLOCK SUPPORTED
IN MAVERICK
64MBYTE TOTAL ADDRESS
SPACE PER block
Block_0
4SRAM BLOCK
SUPPORTED IN
MAVERICK
FIRST 1MBYTE VALID
ADDRESS SPACE PER BLOCK
SUPPORTED IN MAVERICK
Block_1
4SRAM BLOCK SUPPORTED
IN MAVERICK
FIRST 1MBYTE VALID
ADDRESS SPACE PER BLOCK
SUPPORTED IN MAVERICK
Block_2
FIRST 1MBYTE VALID
ADDRESS SPACE PER BLOCK
SUPPORTED IN MAVERICK
4SRAM BLOCK
SUPPORTED IN
MAVERICK
Block_3
Block_4
FLASH MEMORY ADDRESS
SPACE SUPPORTED BY
MAVERICK
Block_5
Block_6
Block_7
ENDING ADDRESS IN
MAVERICK: 32'h6000_0000

FIG. 9

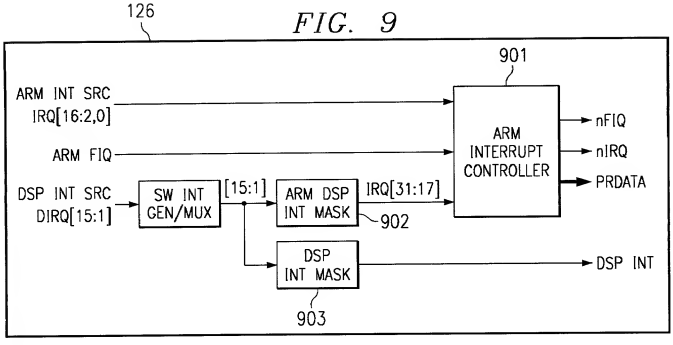
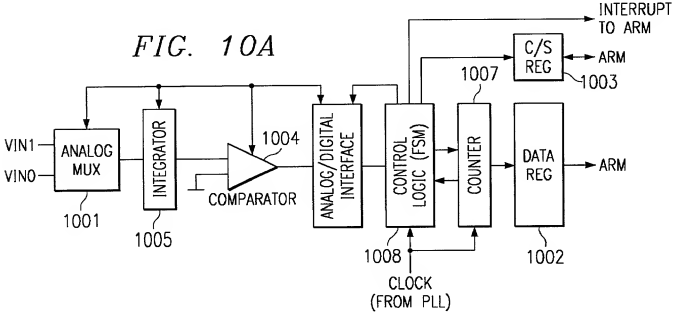

126
901
ARM INT SRC
IRQ[16:2,0]
ARM FIQ
DSP INT SRC
DIRQ[15:1]
SW INT
GEN/MUX
[15:1]
ARM DSP
INT MASK
IRQ[31:17]
902
ARM
INTERRUPT
CONTROLLER
nFIQ
nIRQ
PRDATA
DSP
INT MASK
DSP INT
903

FIG. 10A


INTERRUPT
TO ARM
C/S
REG
ARM
1003
1007
VIN1
VIN0
ANALOG
MUX
1001
INTEGRATOR
1005
1004
COMPARATOR
ANALOG/DIGITAL
INTERFACE
CONTROL
LOGIC (FSM)
COUNTER
DATA
REG
ARM
1008
1002
CLOCK
(FROM PLL)

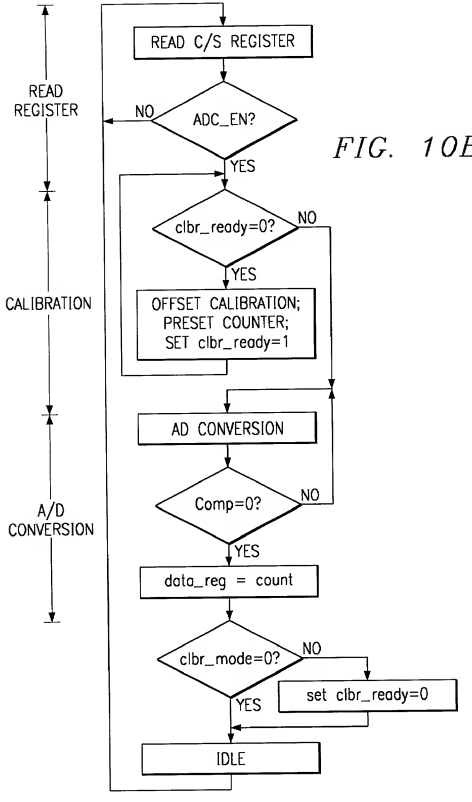

READ REGISTER
CALIBRATION
A/D CONVERSION
READ C/S REGISTER
ADC_EN?
NO
YES
clbr_ready=0?
NO
YES
OFFSET CALIBRATION;
PRESET COUNTER;
SET clbr_ready=1
AD CONVERSION
Comp=0?
NO
YES
data_reg = count
clbr_mode=0?
NO
YES
set clbr_ready=0
IDLE

FIG. 10B

FIG. 11A

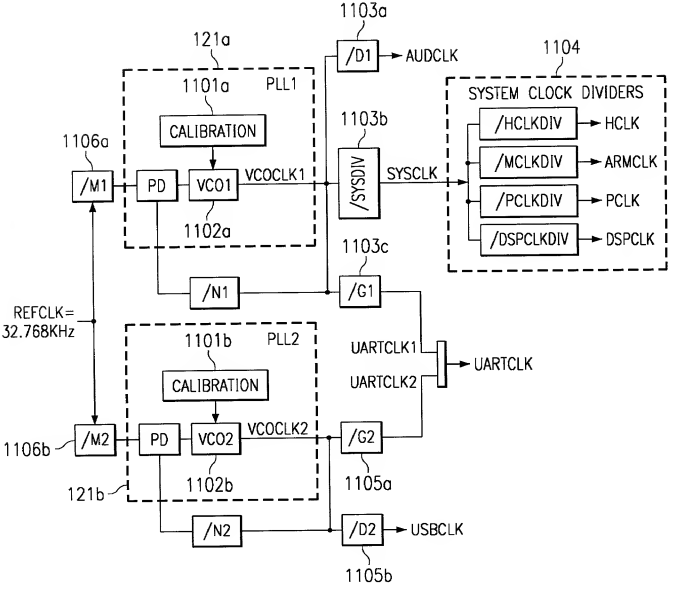

1103a
/D1
AUDCLK
1104
SYSTEM CLOCK DIVIDERS
121a
1101a
PLL1
CALIBRATION
1103b
/SYSDIV
SYSCLK
/HCLKDIV
HCLK
/MCLKDIV
ARMCLK
/PCLKDIV
PCLK
/DSPCLKDIV
DSPCLK
1106a
/M1
PD
VCO1
VCOCLK1
1102a
1103c
/N1
/G1
REFCLK=
32.768KHz
1101b
PLL2
UARTCLK1
UARTCLK2
UARTCLK
CALIBRATION
1106b
/M2
PD
VCO2
VCOCLK2
/G2
1102b
1105a
121b
/N2
/D2
USBCLK
1105b

FIG. 11B

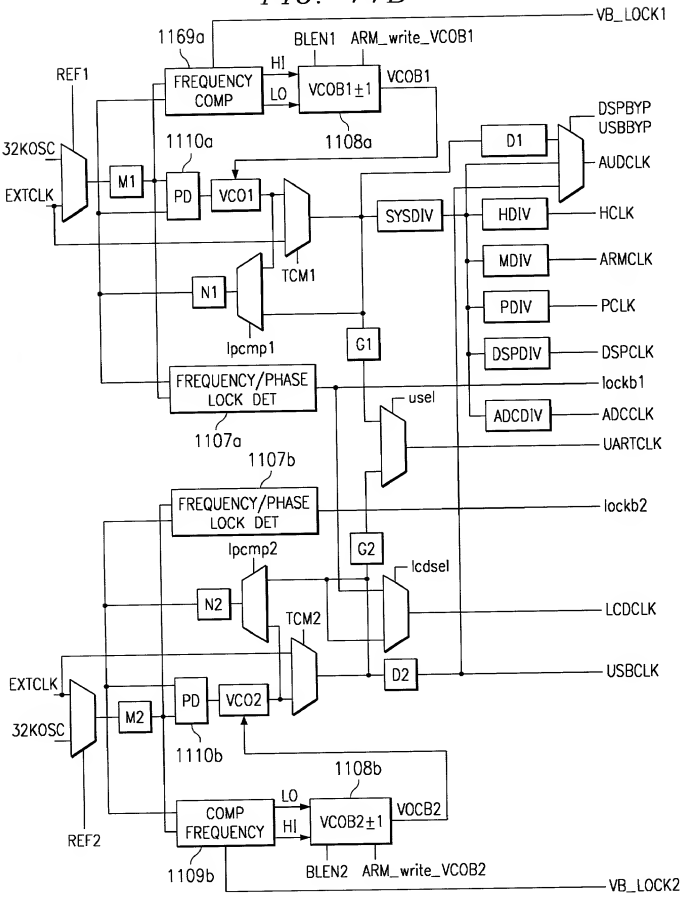

VB_LOCK1
1169a
BLEN1
ARM_write_VCOB1
REF1
FREQUENCY COMP
HI
LO
VCOB1±1
VCOB1
1108a
DSPBYP
USBBYP
D1
AUDCLK
32KOSC
1110a
EXTCLK
M1
PD
VCO1
SYSDIV
HDIV
HCLK
TCM1
MDIV
ARMCLK
N1
PDIV
PCLK
lpcmp1
G1
DSPDIV
DSPCLK
FREQUENCY/PHASE LOCK DET
lockb1
usel
ADCDIV
ADCCLK
1107a
UARTCLK
1107b
FREQUENCY/PHASE LOCK DET
lockb2
lpcmp2
G2
lcdsel
N2
TCM2
LCDCLK
D2
USBCLK
EXTCLK
PD
VCO2
M2
32KOSC
1110b
1108b
LO
COMP FREQUENCY
HI
VCOB2±1
VOCB2
REF2
1109b
BLEN2
ARM_write_VCOB2
VB_LOCK2

FIG. 11C

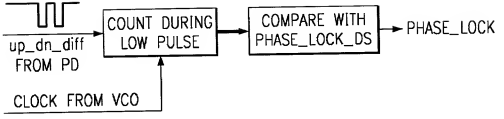


FIG. 11D

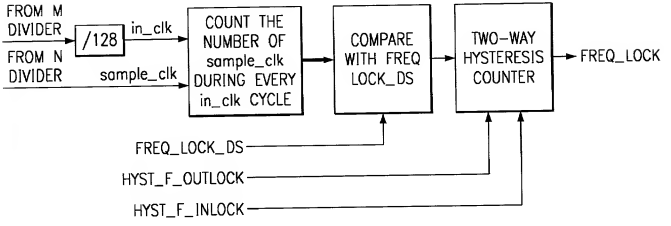


FIG. 12A

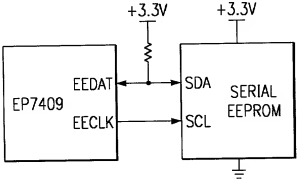
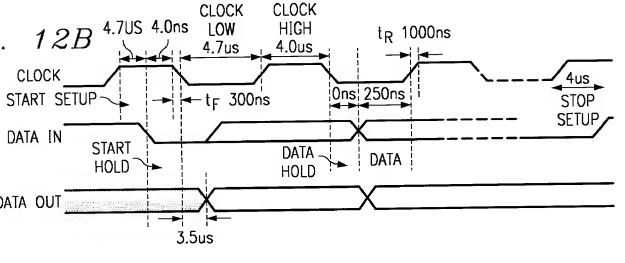


FIG. 12B



7007CD" 2CBT2BCC

FIG. 12C

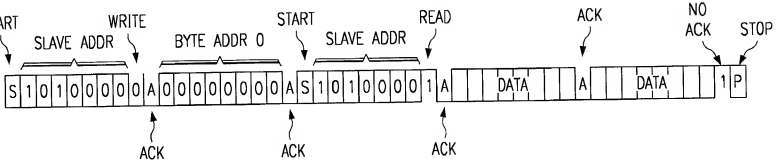
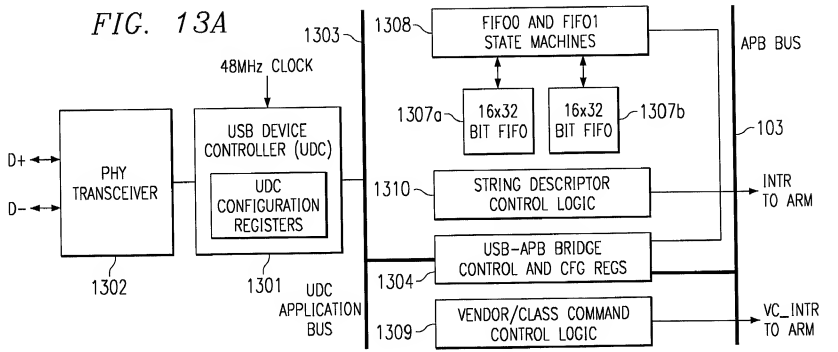


FIG. 13A



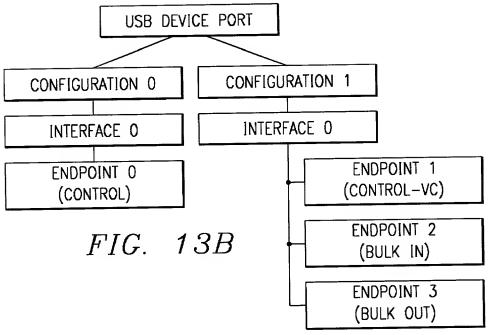


FIG. 13B

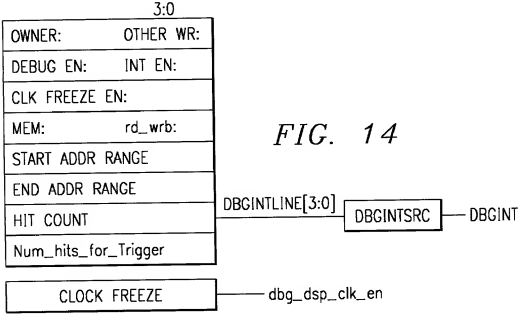


FIG. 14

FIG. 15

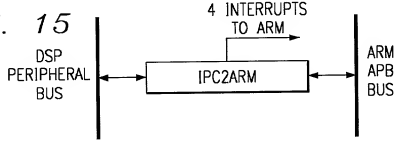


FIG. 16A

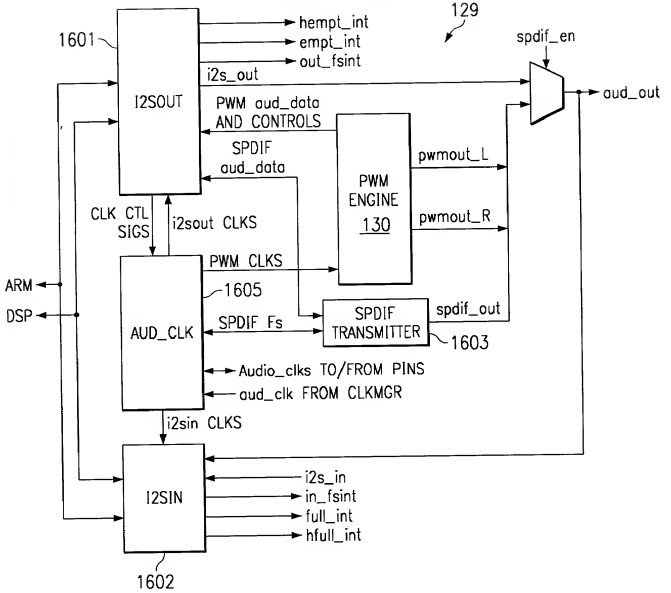

129
1601
hempt_int
empt_int
out_fsint
i2s_out
spdif_en
aud_out
I2SOUT
PWM aud_data
AND CONTROLS
SPDIF
aud_data
PWM
ENGINE
130
pwmout_L
pwmout_R
CLK CTL
SIGS
i2sout CLKS
PWM CLKS
ARM
DSP
1605
AUD_CLK
SPDIF Fs
SPDIF
TRANSMITTER
spdif_out
1603
Audio_clks TO/FROM PINS
aud_clk FROM CLKMGR
i2sin CLKS
I2SIN
i2s_in
in_fsint
full_int
hfull_int
1602

FIG. 16B

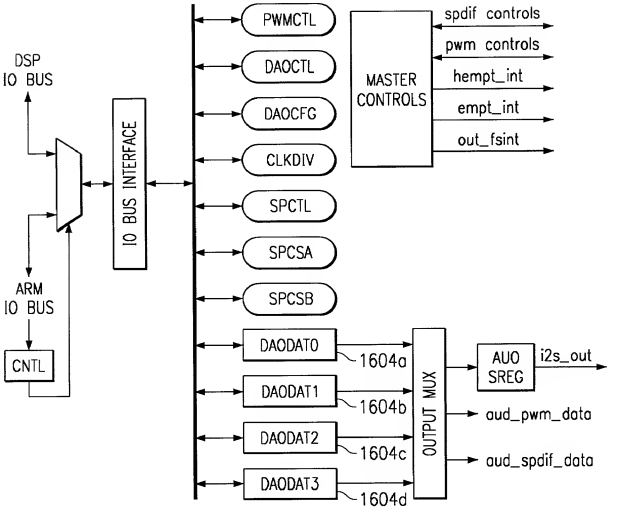


FIG. 16C

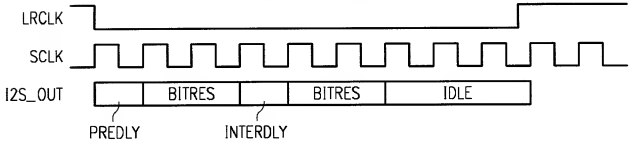


FIG. 16D

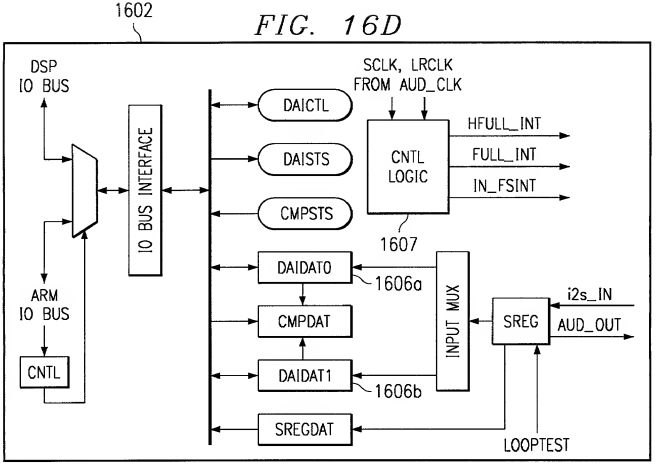
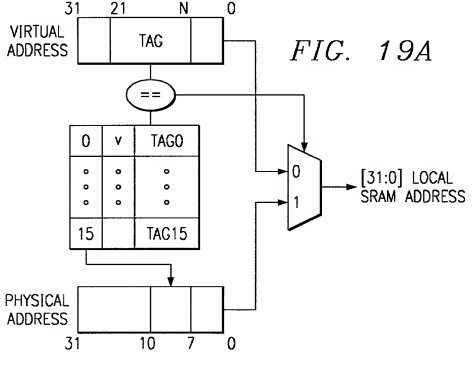


FIG. 19A



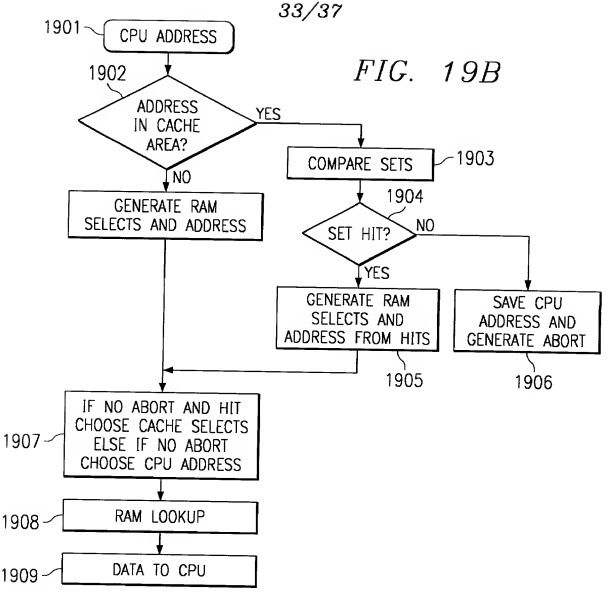


FIG. 19B

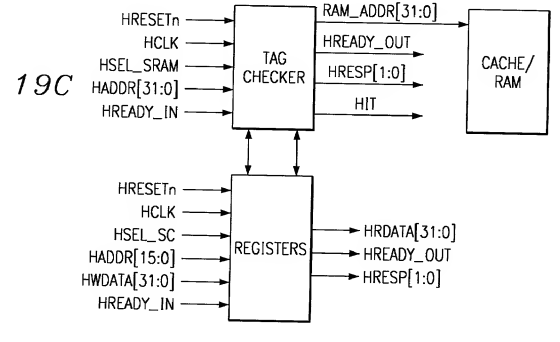


FIG. 19C

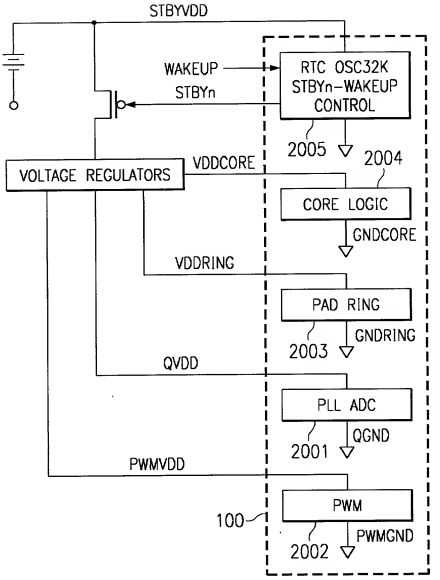


FIG. 20A

FIG. 20B

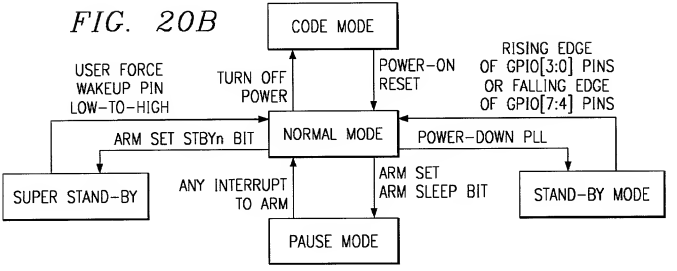


FIG. 20C

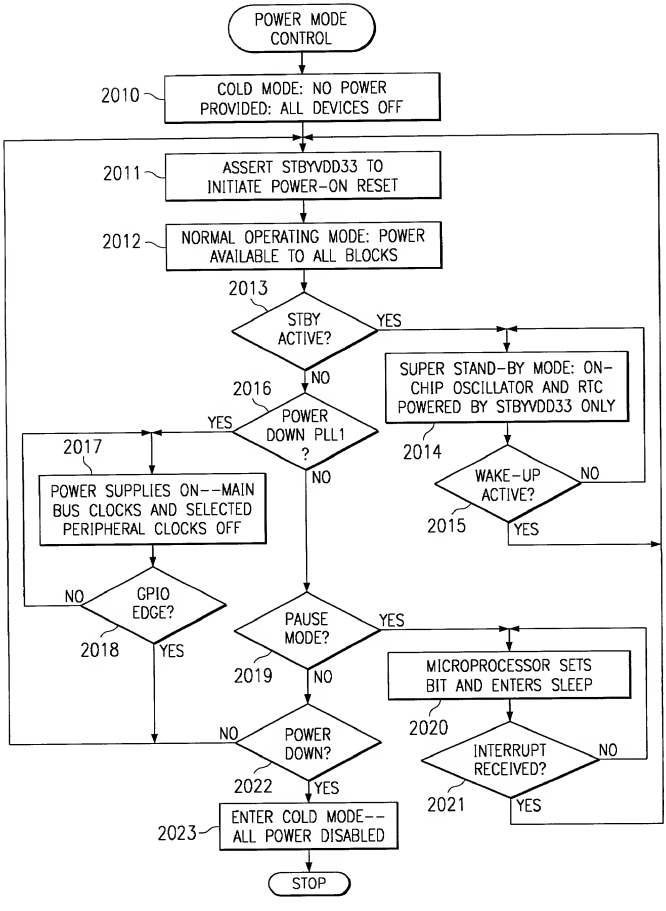
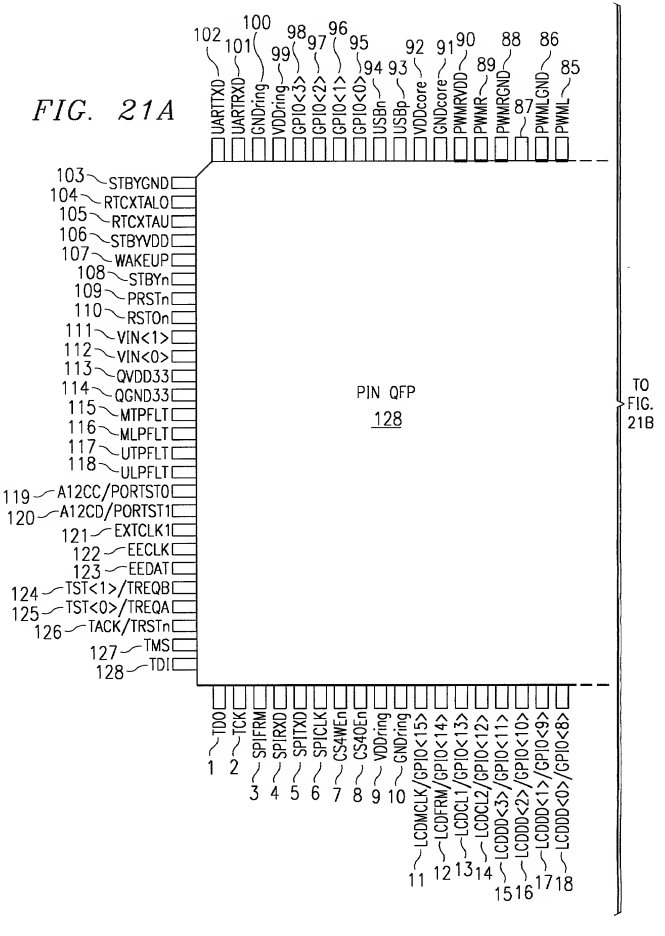

POWER MODE CONTROL
2010
COLD MODE: NO POWER PROVIDED: ALL DEVICES OFF
2011
ASSERT STBYVDD33 TO INITIATE POWER-ON RESET
2012
NORMAL OPERATING MODE: POWER AVAILABLE TO ALL BLOCKS
2013
STBY ACTIVE?
YES
NO
SUPER STAND-BY MODE: ON-CHIP OSCILLATOR AND RTC POWERED BY STBYVDD33 ONLY
2014
2016
POWER DOWN PLL1 ?
YES
NO
2017
POWER SUPPLIES ON--MAIN BUS CLOCKS AND SELECTED PERIPHERAL CLOCKS OFF
WAKE-UP ACTIVE?
NO
2015
YES
NO
GPIO EDGE?
2018
YES
PAUSE MODE?
YES
2019
NO
MICROPROCESSOR SETS BIT AND ENTERS SLEEP
2020
NO
POWER DOWN?
INTERRUPT RECEIVED?
NO
2021
2022
YES
YES
2023
ENTER COLD MODE-- ALL POWER DISABLED
STOP

FIG. 21A


PIN QFP
128
TO FIG. 21B
1 TDO
2 TCK
3 SPIFRM
4 SPIRXD
5 SPITXD
6 SPICLK
7 CS4WEn
8 CS40En
9 VDDring
10 GNDring
11 LCDMCLK/GPIO<15>
12 LCDFRM/GPIO<14>
13 LCDCL1/GPIO<13>
14 LCDCL2/GPIO<12>
15 LCDDD<3>/GPIO<11>
16 LCDDD<2>/GPIO<10>
17 LCDDD<1>/GPIO<9>
18 LCDDD<0>/GPIO<8>
85 PWML
86 PWMLGND
87
88 PWMRGND
89 PWMR
90 PWMRVDD
91 GNDcore
92 VDDcore
93 USBp
94
95 USBn
96 GPIO<1>
97 GPIO<2>
98 GPIO<3>
99 VDDring
100 GNDring
101 UARTRXD
102 UARTTXD
103 STBYGND
104 RTCXTALO
105 RTCXTAU
106 STBYVDD
107 WAKEUP
108 STBYn
109 PRSTn
110 RSTOn
111 VIN<1>
112 VIN<0>
113 QVDD33
114 QGND33
115 MTPFLT
116 MLPFLT
117 UTPFLT
118 ULPFLT
119 A12CC/PORTST0
120 A12CD/PORTST1
121 EXTCLK1
122 EECLK
123 EEDAT
124 TST<1>/TREQB
125 TST<0>/TREQA
126 TACK/TRSTn
127 TMS
128 TDI

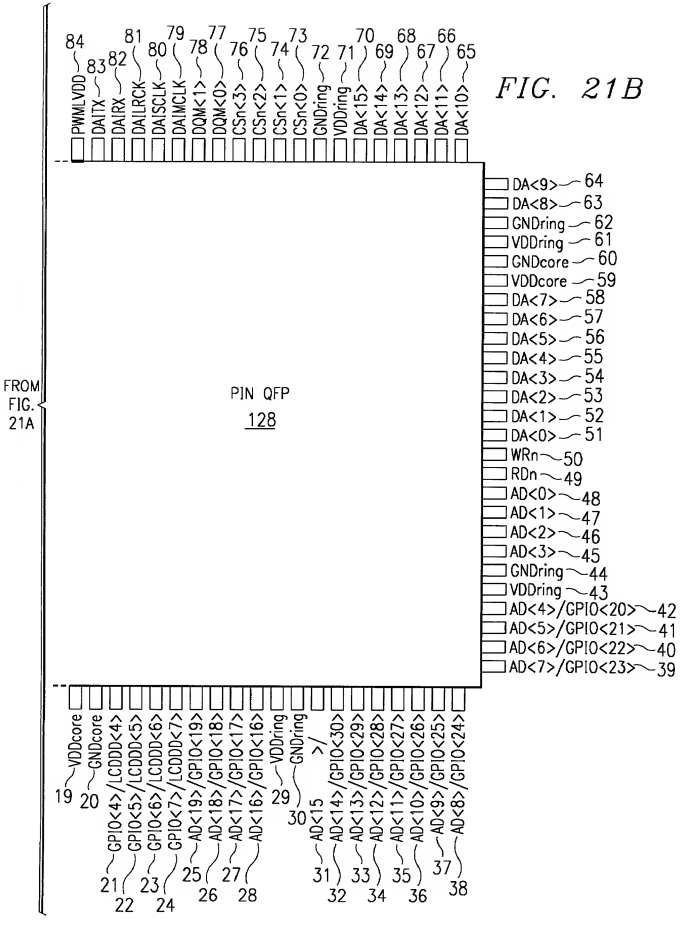

FROM FIG. 21A
PIN QFP 128
84 PWMLVDD
83 DAITX
82 DAIRX
81 DAILRCK
80 DAISCLK
79 DAIMCLK
78 DQM<1>
77 DQM<0>
76 CSn<3>
75 CSn<2>
74 CSn<1>
73 CSn<0>
72 GNDring
71 VDDring
70 DA<15>
69 DA<14>
68 DA<13>
67 DA<12>
66 DA<11>
65 DA<10>
64 DA<9>
63 DA<8>
62 GNDring
61 VDDring
60 GNDcore
59 VDDcore
58 DA<7>
57 DA<6>
56 DA<5>
55 DA<4>
54 DA<3>
53 DA<2>
52 DA<1>
51 DA<0>
50 WRn
49 RDn
48 AD<0>
47 AD<1>
46 AD<2>
45 AD<3>
44 GNDring
43 VDDring
42 AD<4>/GPIO<20>
41 AD<5>/GPIO<21>
40 AD<6>/GPIO<22>
39 AD<7>/GPIO<23>
19 VDDcore
20 GNDcore
21 GPIO<4>/LCDDD<4>
22 GPIO<5>/LCDDD<5>
23 GPIO<6>/LCDDD<6>
24 GPIO<7>/LCDDD<7>
25 AD<19>/GPIO<19>
26 AD<18>/GPIO<18>
27 AD<17>/GPIO<17>
28 AD<16>/GPIO<16>
29 VDDring
30 GNDring
31 AD<15>/GPIO<30>
32 AD<14>/GPIO<29>
33 AD<13>/GPIO<28>
34 AD<12>/GPIO<27>
35 AD<11>/GPIO<26>
36 AD<10>/GPIO<25>
37 AD<9>/GPIO<24>
38 AD<8>/GPIO<23>

FIG. 21B